Abstract: Image decompression involves bit-plane decoding (BPD) followed by the 2-dimensional Inverse Discrete Wavelet Transformation (IDWT). BPD involves DC coefficients decoding and stage 1 to stage 4 AC coefficients decoding. IDWT involves level 3 to level 1 row-wise and column-wise inverse discrete wavelet transformation. In this paper, we present the design of VLSI architecture for CCSDS standard DWT-based image decompression. This architecture has been implemented using Verilog HDL in Xilinx ISE environment. The decompression process is controlled by Xilinx Micro Blaze embedded soft micro-processor. Embedded C code is developed in Xilinx EDK environment. This paper presents an efficient VLSI architecture of BPD and IDWT implemented in Xilinx VIRTEX V ML501.

Keywords: Image Decompression, Bit-Plane Decoding, CCSDS, Micro Blaze, 2-D IDWT, FPGA.

I. INTRODUCTION

With the rapid development of remote sensing technology, the image resolution is becoming higher and higher. Space missions are faced with the necessity of handling an extensive amount of imaging data. Image compression compensates for the limited onboard resources, in terms of mass memory and downlink bandwidth and thus provides a solution to the “bandwidth vs. data volume” dilemma of modern spacecraft. In 2005, Consultative Committee for Space Data Systems (CCSDS) established a Recommended Standard for a data compression algorithm, namely CCSDS 122.0-B-1, Image Data Compression (IDC) standard.

The CCSDS IDC algorithm makes use of Discrete Wavelet Transform (DWT) to reach high compression ratio and high visual quality. There are also some other DWT-based image compression algorithms, for instance JPEG2000, SPIHT and No-List SPIHT algorithm. JPEG2000 has high compression performance but its high complexity makes it too difficult to implement in space application. SPIHT algorithm employs three lists to store significant information which consumes lots of memory. No-list SPIHT algorithm reduces the memory size but it has lower compression performance comparing with SPIHT. The CCSDS IDC algorithm differs from image compression algorithm mentioned above in several respects. It specially targets spacecraft instruments having high bit-rates and its low complexity supports fast and low power hardware implementation. Because of these advantages, CCSDS algorithm is becoming more and more popular in space applications. It consists of two functional parts, a DWT module and a Bit-Plane Encoder (BPE) which encodes the transformed data. Performance of these modules is critical for good quality data availability from the instruments. This paper presents an efficient VLSI architecture for image decompression, which consists of the reverse process - Bit Plane Decoding followed by Inverse Discrete Wavelet Transform. Field Programmable Gate Array (FPGA) is a flight-proven hardware platform for high performance computing, as it has been used in a number of space missions. The proposed architecture of BPD and IDWT has been implemented in Xilinx Virtex-5 FPGA. The two individual IPs are created and the entire action is controlled by using an embedded Xilinx Micro Blaze processor. The whole architecture is implemented on Xilinx ML501 evaluation platform board.

II. IMAGE DECOMPRESSION

The compression process consists of two functional parts, 3-level 2-dimensional Discrete Wavelet Transform followed by Bit Plane Encoding. At the receiving side, the process is reversed: Bit Plane Decoding followed by 3-level 2-dimensional Inverse Discrete Wavelet Transform. The DWT analysis filter consists of nine and seven taps for low-pass and high-pass filters to de-correlate image data. Bit Plane Decoding consists of DC coefficients decoding using the Rice algorithm followed by AC coefficients
decoding. The data flow for decompression is shown in Figure 1.

![Image](image1.png)

Figure 1: Image decompression flow

**A) Bit Plane Decoding:**
Wavelet coefficients after 3-level decomposition are arranged into blocks and segments. A block consists of 1 DC coefficient and its corresponding 63 AC coefficients. The organization of the coefficients within a block is as shown in Figure 2.

![Image](image2.png)

Figure 2: Block components after DWT

A group of 16 or more blocks constitutes one segment. DWT Coefficients are encoded by the Bit-Plane Encoder segment by segment.

Bit Plane Decoder consists of DC coefficients Decoder which performs initial decoding of DC coefficients followed by AC coefficients decoding. DC decoder reads the Bit Depth DC header field, and applies RICE algorithm to decode the compressed DC coefficients. The same algorithm meant for unsigned coefficients is used to decode the AC bit-depth values for each block. AC decoder processes the coefficients in three steps: it begins with coefficients significance scanned, then decodes bit planes of significance information from most-significant bit plane to least-significant bit plane, and finally entropy decodes the words by using variable-length binary codes.

**B) Inverse Discrete Wavelet Transform:**
There are two specific wavelets in CCSDS standard: the 9/7 biorthogonal DWT, referred to as Float DWT, and a non-linear, integer approximation to this transform, referred to as Integer DWT. The Float DWT can obtain superior performance in the lossy domain, but only the Integer DWT supports strictly lossless compression. The lifting scheme is suited for hardware implementation of DWT. It is constituted of prediction and updating steps as shown in Figure 3.

![Image](image3.png)

Figure 3: DWT and IDWT flow

The advantage of lifting scheme is the forward and inverse transform are obtained from the same architecture. Here $k$ is the constant of normalization in
the steps of prediction and the updating at decomposition in poly phase matrix.
The poly phase representation of a discrete filter \( h(n) \) is defined as:

\[
H(z) = H_e(z) + \frac{1}{z} H_o(z)
\]  

(1)

Where \( H_e(z) \) and \( H_o(z) \) represent the filters obtained using the even and odd coefficients respectively. If we represent \( h(z) \) and \( g(z) \), the low pass and high pass coefficients of the synthesis filters, the poly phase matrix can be written as:

\[
P(z) = \begin{bmatrix} h_e(z) & g_e(z) \\ h_o(z) & g_o(z) \end{bmatrix}
\]  

(2)

The filters \( h_e(z) \), \( h_o(z) \), \( g_e(z) \) and \( g_o(z) \) are Laurent polynomials. As the set of all polynomials exhibits a commutative ring structure, within which polynomial division with remainder is possible, long division between two Laurent polynomials is not a unique operation. In Euclidean algorithm decomposition can be used, and the poly Phasor \( P(z) \) is finally obtained as:

\[
P(z) = \frac{1}{k} \begin{bmatrix} s_i(z) \\ t_i(z) \end{bmatrix}
\]  

\[
\begin{bmatrix} 1 & 0 \\ 1 & 1/k \end{bmatrix}
\]  

(3)

Where \( s_i(z) \) and \( t_i(z) \) are primal lifting and dual lifting filters respectively, and \( k \) is a constant of normalization at low and high coefficients filters. The 5/3 wavelet filter transform is more suitable for lossless data compression adopted in JPEG2000, and 9/7 filter is used in JPEG2000 for lossy compression data. The 5/3 filter has one prediction and one up-dating compared to two predictions and two up-dating for 9/7 filter. The following steps are necessary to get their wavelet: Split the input signal into coefficients at odd and even positions, perform a predict step, and then perform update step.

**Forward DWT:**

\[
s(0) = s_{21}
\]

\[
s(0) = s_{21+1}
\]

\[
d(1) = dl(0) - \frac{-1}{16} (s(0)_{t-1} + s(0)_{j+2})
\]

\[
+ \frac{9}{16} (s(0)_{t-0} + s(0)_{j+1}) + \frac{1}{2}
\]

\[
s(1) = sl(0) - \frac{1}{4} (d(1)_{t-1} + d(1)_{j}) + \frac{1}{2}
\]

**Backward DWT (IDWT):**

\[
s(0) = sl(1) + \frac{-1}{4} (d(1)_{t-1} + d(1)_{j}) + \frac{1}{2}
\]

\[
s_{21+1} = dl(0)
\]

\[
s_{21} = sl(0)
\]

The lifting based implementation of DWT/IDWT is shown in Fig.3.

**C) 2D Single level DWT:**

Image de-correlation is accomplished using 2D DWT, and it is performed on the image using two 1-D DWT. The 1-D DWT is applied on each image row producing a horizontal low-pass and a horizontal high-pass filtered intermediate data array and reducing the width by half. The same action is performed on the column of both intermediate data arrays to produce four sub bands with the width decreased by half each. Now the four sub bands are the LL, HL, HH and LH.

**D) Inverse 2D DWT:**

This can be obtained by repeating the 1-DIDWT operations multiple times to get back to the original image. First each column is inverted to produce the intermediate transform data arrays. The 1-D IDWT is applied to the LL and the LH sub bands first and then the 1-DIDWTs are applied in column wise for the sub bands HL and HH. Both resulting in its intermediate values. The 1-D DWT inverse is applied to rows of the intermediate horizontal low pass and horizontal high
pass array to get back the original image. This mechanism is followed for all the three levels.

III. VLSI ARCHITECTURE FOR BIT PLANE DECODER

The data is received from the satellite in the strip based form. The stream consists of the segment header followed by the coded compressed bits after the Bit Plane Encoding. The information received from the segment header is decoded and the corresponding DC and AC Bit Plane Decoder settings are set, and the process of decoding starts.

A) DC Decoder:

When the data is received in the form of the compressed bit stream, it also includes the segment header. The type of information and the coded format is specified, and based on that the decoding is performed. Once the data is identified as DC coefficients, the data that is received is scanned and based on the Bit Depth DC value, the DC decoding is performed. The DC decoding consists of Rice decoding. DC decoding consists of 2 parts: Adaptive Entropy decoding, followed by Post processing, as shown in Figure 5.

B) AC Decoder:

The AC decoder performs bit plane decoding and it is the most complex part that constrains the throughput performance. The high-level VLSI architecture of AC decoder is illustrated.

It consists of five functional parts: coefficients position demap module, significance scan module, words extraction module, symbols demap module and entropy decoder module. The high-level architecture is illustrated in figure 6. Stage-1 decodes the Parent coefficients, Stage-2 the Children coefficients, and Stage-3 the Grandchildren coefficients. Stage-4 is for refinement and it works on all the coefficients. The compressed words are extracted using Word Extraction module which interfaces with Bit-stream reader.

i) Entropy decoder module:

The entropy encoding is adopted to improve the compression performance in the CCSDS standard. The entropy decoder decodes the bit plane bits, and in the bit stream we have only the higher bit planes in extreme situations. The symbols are decoded using variable lengths binary words. Entropy decoding is performed in units of gaggles. There are 16 bit planes. In order to improve the entropy decoding efficiency, all words and symbols in the dual port RAM shall be read out but only words and symbols with length greater than zero shall be written back into the RAM. In this way, all the valid symbols are stored in the RAM consecutively and the time for entropy decoding is decreased greatly and the original coefficients are obtained.

ii) Symbols de-map module:

The symbols are stored in the dual port ram at each bit plane. The mapping table is stored in the ROM. The words which are greater than 1 word are mapped to integer value referred to as symbols. There are 38 transaction and 21 words at most are mapped to the symbols so whenever the symbols is matched with the data the corresponding data is replaced. The signed bit words and the words of length 1 bits are not coded so they remain the same. The long words are to be decoded by 1 sign bit word together form the long word which should be decoded. The two bit planes share one symbol map module and all the symbols are mapped to words.

IV. VLSI ARCHITECTURE OF IDWT

The input to the IDWT module is the output of the Bit Plane Decoding that is the de-correlated output. The DWT that is performed at the compression side is of 3 stages, so the resultant sub-bands obtained are 10, and for every row and column 1-DDWT is performed, and the size gets halved at each stage.

We have chosen two BRAMs to store the high pass coefficients and the low pass coefficients in two separate memory block which can also be called as on-chip buffers, which feed the values to the IDWT
module. This module computes the data and stores the resultant data in the other BRAM. This BRAM is mapped to DDR2-SDRAM and BRAM gets ready for the next batch of coefficients.

The VLSI architect is designed in such a way that 2DIDWT is split into two 1-D-IDWT modules, once for a rows and then the columns. This IDWT module is made into an intellectual property which is linked to the Micro Blaze processor. The entire module is divided into two modules: the top module of the IDWT and the 1-D-IDWTmodule. The 1-DIDWTmodule is the sub module which is called by the IDWT top module. The IDWT sub module is fed with two inputs of data: the low-pass values and the high-pass values, and one start signal which will enable the sub module. When the start is enabled in sub module the 1-DIDWT is performed by implementing the update and the predict module as shown in fig 9. The update and predict modules also have boundary condition for which we use a counter and arrange the boundary condition computation on the data. The data is fed into the memory at half the clock rate, and the data is read out as a merged data for which we run a counter and the data is read out of the module to the top module. The signals out of this module are the done signal, address of the data that is to be fed to the module and the data that is read out.

sets. Now we have to perform the row wise operations, i.e., the data to the 1-D-IDWT is read row wise and the same flow goes on till all the column values are read from the memory and the counter gets incremented for every done signal received from the IDWT sub-module. Once the IDWT is completed the data is now ready for the second decomposition and the entire flow goes on the row wise and the column wise computations structure is shown is Fig 8.

![Figure 7: IDWT 3 level decomposition](image7.png)

When we send the done signal to the top module, the next set of column values are sent to the sub modules. In order to control the number of values sent, we have a count of columns. Once all the columns are sent to the sub modules, we have the values of vertical filter in two

![Figure 8: Row-wise and Column-wise Single-level 2-DIDWT](image8.png)

![Figure 9: Update, predict operations in 1-D-IDWT](image9.png)
V. SOC ARCHITECTURE FOR BIT PLANE DECODER AND IDWT

SoC is the term for System on Chip which is the integration of all the components into a single chip. The board used for decompression is Xilinx ML501. The system clock of this board is 100 MHz and this is the clock with which the system is operated. The SoC consists of the Micro Blaze processor which has two ports: the ILMB (instruction LMB) and the DLMB (data LMB) connected to the PLB bus. The data that is received from the satellite is the compressed bit stream. This bit stream consists of a header followed by the compressed encoded bits. The Micro Blaze reads the values from the segment header and configures the BPD and also the data that is to be read from the memory. The segment header consists of all the information which is related to the data that is present following the Bit Plane Decoder. All the preprocessing is done by the Micro Blaze processor. The data arranged in the segment is read out from the memory by the Micro Blaze processor. In the decompression side, the Bit Plane Decoder and the IDWT are performed respectively for which we have designed two intellectual properties. Now for these two intellectual properties we have designed two controllers one for the BPD and the other for the IDWT, which is connected by the ILMB and the DLMB cables internally. The Micro Blaze on the whole is connected to the PLB bus. This bus also connects the two IP controllers which we have designed and also the DDR2-SDRAM controller which is where access the data and store back the data. The Bit Plane Decoding is performed first and once all the data is read and arranged into 10 sub bands in the BRAM memory then we initiate the IDWT module and finally the end data is stored back and send into a file. This architecture is shown in Fig 10.

VI. EXPERIMENTAL RESULTS

The proposed architecture is coded using Verilog HDL. The design has been implemented in the Xilinx VIRTEX V ML 501 FPGA using the Xilinx Integrated Software Environment (ISE) 14.4 version.

Table 1: Compression Ratio (bits / pixel)

<table>
<thead>
<tr>
<th>Bit depth</th>
<th>Image</th>
<th>CCSDS</th>
<th>CCSDS/RICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Europa3</td>
<td>6.61</td>
<td>7.48</td>
</tr>
<tr>
<td>8</td>
<td>lunar</td>
<td>4.58</td>
<td>5.23</td>
</tr>
<tr>
<td>12</td>
<td>solar</td>
<td>6.21</td>
<td>7.12</td>
</tr>
<tr>
<td>12</td>
<td>Sunspot</td>
<td>5.79</td>
<td>6.63</td>
</tr>
</tbody>
</table>

Table 2: Results of the architecture designed

<table>
<thead>
<tr>
<th>Parameters</th>
<th>used</th>
<th>Available</th>
<th>Utilized</th>
</tr>
</thead>
<tbody>
<tr>
<td>No of slices</td>
<td>12992</td>
<td>28200</td>
<td>46%</td>
</tr>
<tr>
<td>No of slices flipflops</td>
<td>11731</td>
<td>28200</td>
<td>55%</td>
</tr>
<tr>
<td>Number of 4-input LUTs</td>
<td>17940</td>
<td>28200</td>
<td>63%</td>
</tr>
<tr>
<td>No of BRAMs</td>
<td>41</td>
<td>60</td>
<td>68%</td>
</tr>
<tr>
<td>Frequency of Operation</td>
<td>100 MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Xilinx Platform Studio is used to build the system. The operating frequency of the architecture can be up to 120 MHz but in the implementation of the design has been performed in 100MHz. Eclipse software development tool is used to program the Micro Blaze. The average compression ratio for CCSDS / Rice method that has been obtained is 6.28 bits/pixels, which is the maximum compression possible, which is shown in the Table 1. The detailed parameters of our FPGA implementation are listed in Table 2.

**VII. CONCLUSION**

In this paper, an efficient VLSI architecture of 3-level 2-D IDWT based on CCSDS IDC is presented. This architecture’s throughput performance is up to 100 M samples/s with the parallel bit plane decoding method and inverse discrete wavelet transform. In order to reduce the resource consumption of parallel architecture, pipeline technology is utilized in three functional parts of the bit plane coding module and once the BPD is done the IDWT is performed. By these means, lots of hardware resource is economized and the architecture is implemented in the Xilinx VIRTEX V ML501 FPGA.

**REFERENCES**

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