**A 12-BIT 7TH ORDER SIGMA DELTA MODULATOR FOR EMBEDDED FPGA APPLICATIONS**

*P.A. Harsha Vardhini*  
Department of ECE, Vignan Institute of Technology and Sciences Deshmukhi, Nalgonda Dist., India.

**Abstract:** This paper proposes a 12-bit 7th order sigma delta modulator designed to work at a signal band of 20 KHz at an OSR of 64 with a sampling frequency of 2.56 MHz Modulator is implemented in MATLAB & VHDL. The complete Sigma Delta ADC, consisting of analog block of 7th order modulator and digital block of decimator consumes a total power 0.052W which is suitable for embedded FPGA applications. The stability analysis is based on the modeling the quantizer for each clock period at a time. The quantizer’s gain in the modulator at the present clock period determines the modulator’s stability for the next clock period. If the modulator is stable during each clock period, it is unconditionally stable and behaves as a linear analog to digital converter.

**Keywords:** Sigma Delta Modulator; FPGA; ADC; FFT; Decimator.

**I. INTRODUCTION**

Data Converters – Analog to Digital Converters or digital to Analog Converters are the most essential modules in any system. Sigma delta modulation technique with simple analog components and digital signal processing can perform both analog to digital and digital to analog conversion to achieve high accuracy and immunity to component errors [1]. A basic premise of sigma-delta modulation is that the sampling rate is much greater than the highest frequency of interest present in the input. This paper proposes the design of sigma delta ADC which is suitable for embedded FPGA applications. FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform.

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"— somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. To define the behavior of the FPGA, the user provides a hardware description language (HDL) or a schematic design. The HDL form might be easier to work with when handling large structures because it’s possible to just specify them numerically rather than having to draw every piece by hand. On the other hand, schematic entry can allow for easier visualization of a design. Section II details the 7th order SDM architecture. Section III illustrates the MATLAB and VHDL simulations and the corresponding results. Section IV concludes the paper.

**II. 7TH ORDER SIGMA DELTA MODULATOR**

The analog inputs are continuously sampled by the analog modulators, eliminating the need for external sample and hold circuitry. The input information is contained in the output stream as a density of ones. The original information can be reconstructed with an appropriate digital filter.

![Diagram of Sigma delta modulator](image)

**Figure 1:** Block diagram of Sigma delta modulator

ADC

The 7th order Sigma Delta Modulator is cascade of two MOD1 Sigma Delta Modulators. The input information is contained in the output stream as a density of ones. The analog inputs are continuously sampled by the analog modulators, eliminating the need for external sample and hold circuitry. The input information is contained in the output stream as a density of ones. The original information can be reconstructed with an appropriate digital filter.

The block diagram of a 7th order sigma delta modulator consists of a integrators, comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The integrator in the circuit, placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted from the input signal of the integrator. Similarly, when the integrator output is negative, the comparator feeds back a negative signal that is added to the incoming signal.

The integrator therefore accumulates the difference between the input and quantized output signals from the DAC output which is in feedback loop and makes the integrator output around zero. A zero integrator output implies that the difference between the input signal and the quantized output is zero. Oversampling analog to digital converters generally use switched-capacitor techniques and hence do not use sample
and hold circuits unlike in other ADC architectures. The output of the modulator is a pulse density modulated signal that represents the average of the input signals [2,3].

III. SIMULATIONS AND RESULTS

A) MATLAB Simulation Results

Simulations are carried out in MATLAB and are shown below. Fig. 3 depicts the input sine wave of 50 KHz applied to the MOD7 SDM and the corresponding output is shown in

![Figure 2: Block diagram of 7th order Sigma Delta modulator](image)

![Figure 3: Input to MOD7 Sigma Delta Modulator](image)

![Figure 4: Output of MOD 7 sigma delta modulator](image)

Fig. 4, Fig. 5 and Fig. 6 depict the FFT for the given input and the FFT of the output of MOD7 SDM respectively. The spectrum shown in Fig.6 represents the FFT of MOD7 output exhibits a noise-shaped characteristic. At low frequencies, the NTF of MOD7 has a 40 db/decade slope. The increased attenuation at frequencies close to dc is desirable because it reduces the amount of quantization noise within the signal band [4]. Unfortunately, since the gain at high frequencies provided by MOD7’s NTF is greater than that of MOD1’s NTF, the total power of the quantization noise at the output of MOD7 is more than that of MOD1.

Fig. 7 illustrates the input and output waveforms for MOD7 with a half-scale sine-wave input. As it is typical in delta sigma systems, these waveforms provide very little insight into the system’s behavior when viewed in the time domain. Only crude observation can be made, such as the increased tendency for the output to be +1 when the input is positive and -1 when the input is negative.

B) VHDL Simulation Results

Fig.8 shows the VHDL simulation result for the Adder. Here we are adding two 12 bits inputs A and B. When the clock signal is high the inputs A and B are added and the result is stored in the output signal named SUM. Here the addition is performed in the 2’s complement method.

![Figure 5: FFT of input sine wave](image)

![Figure 6: FFT of MOD7 SDM output](image)

![Figure 7: Output vs. Input MOD7 sigma delta modulator](image)
With the 2’s complement method, subtraction is done and the VHDL simulation results are illustrated in Fig.9. The Fig.10 shows the VHDL simulation result of D Flip-Flop. When the reset is forced one ‘1’ the D flip-flop is cleared with all zero’s and when the reset is zero ‘0’ and the clock is high then the input is delayed for one clock cycle and appear at the output. Fig.11 shows the result of the quantizer. It is a two level quantizer, +1 and -1 are the two levels. When the input is below zero ‘0’ then the output is set to ‘-1’ and when the input is greater than zero ‘0’ then the output is set to ‘+1’.

The Fig. 12 shows the results of the VHDL simulation of MOD7 Sigma Delta Modulator. Here we can see that the test bench generates the system clock and the input sine-wave which is given as input to the MOD7 Sigma Delta Modulator. And also we can see the results at various blocks like adders, subtractors, D flip-flops and quantizer. The output of the MOD7 Sigma-Delta Modulator which is at quantizer output can be seen that it is at two levels +1 and -1 depending on the input signal. Hardware utilization of Spartan 3 is described in Table I.
Table I. Device Utilization using Spartan 3

<table>
<thead>
<tr>
<th>Logic Unit</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slices</td>
<td>236</td>
<td>4656</td>
<td>5%</td>
</tr>
<tr>
<td>Number of Slice Flip Flops</td>
<td>428</td>
<td>9312</td>
<td>4%</td>
</tr>
<tr>
<td>Number of 4 input LUTs</td>
<td>173</td>
<td>9312</td>
<td>1%</td>
</tr>
<tr>
<td>Number of IOBs</td>
<td>26</td>
<td>232</td>
<td>11%</td>
</tr>
<tr>
<td>Number of GCLKs</td>
<td>1</td>
<td>24</td>
<td>4%</td>
</tr>
</tbody>
</table>

IV. CONCLUSION
A sigma delta ADC is designed using a seventh order SD modulator with high resolution. The output of the decimator is a 12-bit digital output with a clock frequency ranging from 256 kHz to 5.12 MHz and the corresponding input signal band of 20KHz. The analog equivalent calculated from the multi bit digital output of the decimator is found to be almost equal to that of input analog sine wave value. Using efficient circuit design techniques the power consumption is minimized to a value of 0.052W.

REFERENCES