ANALYSIS AND SIMULATION OF A SHUNT ACTIVE FILTER TO SOLVE HARMONICS PROBLEMS

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Abstract: - The active power filter has been proved to be an effective method to mitigate harmonic currents generated by nonlinear loads as well as to compensate reactive power. The methods of harmonic current detection play a crucial part in the performance of active power filter (APF). The main objective of this paper is to model a new shunt active power filter using a multi-level inverter for both harmonic filtering and reactive power (var). In this paper, the shunt active power filters are designed using a three-phase, cascade-inverter in MATLAB (using power system Simulink tools).

Keywords: shunt active power filter, inverter, THD, PWM.

I. INTRODUCTION

In recent decades, there are many studies about harmonic distortion with techniques to improve power quality. The harmonic is defined in many literatures as “a component of a periodic wave having a frequency that is an integral multiple of the fundamental power line frequency”. Shunt active power filter (SAPF) is commonly used as an effective method in compensating harmonic components in non-linear loads. Fig. 1 shows the basic principle of SAPF in which APF is connected in parallel to the power system at a point of common coupling (PCC) between metropolitan electricity authority (MEA) and power users. The objective of SAPF is to minimize the distortion in power supply using four main components – harmonic detection, compensating current control, DC bus voltage control, and active power filter.

II. PROPOSED CONTROL STRATEGIES

In this section, the proposed new shunt APF using a three-phase 7-level cascaded voltage source inverter is presented for getting high quality of source voltages and currents waveforms to the same distorted power system utility as taken in the previous section. This section focuses on modeling of a new shunt active power filter and reveals a new switching angle control method for dc voltage balancing of 7-level cascade inverters.

Analysis and Modeling of a New Shunt APF

The 7-level cascaded-inverter is connected to the power distribution system through a small filter, L and C. The control block diagram for the shunt APF is shown in Figure 2. To compensate for reactive and harmonic current, the load current I is sensed, and its reactive and harmonic components are extracted. The current reference I can be the load reactive current component, harmonic component, or both, depending upon the compensation objectives. The cascade inverter has to provide a voltage V so that the filter current IC tracks the current reference I. V is the line terminal voltage, and K is a gain. In a distribution system, the purpose of a shunt active power filter is to provide a constant and stable terminal voltage to loads. In this case, a constant sine wave is assigned to the voltage reference V. A 7-level multilevel inverter consists of own separate dc-bus capacitor source. This new inverter can make
possible direct connection to the 240 V, 50 Hz distribution system in parallel without any additional transformer. By using MATLAB Simulink tools the modeling of a new shunt active power filter implemented by 7-level cascaded-inverter. A series reactance is required for coupling to the ac system. This required reactance can be naturally provided by leakage inductance of the service transformer that already exists in the power system. Each phase of the cascade inverter consists of five H-bridge inverter units in series. With this structure, any voltage level is easy to obtain by increasing the number of inverter units.

![Figure 2: Control block diagram of SAPF](image)

### III. COMPENSATION PRINCIPLE OF SHUNT PASSIVE FILTER

A passive shunt filter consists of several LCR branches each tuned at particular frequency. Figure 3 shows the equivalent circuit diagram of a passive shunt filter. The compensation principle of LC passive shunt filter is as follows:

\[
\frac{I_s}{V_1} = \frac{Z_{sh}}{Z_s Z_e + Z_{sh} + Z_e Z_{sh}}
\]

Where \( Z_{sh} \) is the impedance of the parallel LC filter from (1) it can be seen that the performance of parallel LC filter depends on the source impedance and is determined only by the ratio of the source impedance and the filter impedance. If \( Z_s = 0 \), then \( I_s = I_1 \), which means that the passive filter is not effective. But if \( Z_s = 0 \), then

\[
\frac{I_s}{V_1} = \frac{1}{Z_e}
\]

Which means that the filter does not provide harmonic compensation it is seen that the filter interaction with the source impedance results in a parallel resonance for inductive source impedance \( Z_s \), this occurs at a frequency below the frequency at which the filter is tuned. It is as follows:

\[
f_{sys} = \frac{1}{2\pi(L_s + L)C}
\]

If the filter is tuned exactly at a concern frequency then an upward shift in the tuned frequency results in a sharp increase in impedance as seen by the harmonic. There are some common mechanisms which may cause filter detuning. They are as follows:

- Capacitor fuse-blowing, which lowers the total capacitance, thereby raising the frequency at the filter has been tuned.
- Temperature variation
- System parameter variation
- Manufacturing tolerances in both inductor as well as capacitor.

So the filter banks are tuned to around 6% below the desired frequency as per IEEE standard 1531.

![Figure 3: Equivalent circuit diagram of passive shunt filter based configuration](image)

### Design of shunt passive filter

The passive shunt filter consists of first order series tuned low pass filters tuned for 5\(^{th}\) and 7\(^{th}\) harmonics and a second order damped high pass filter tuned for 11\(^{th}\) harmonics.

#### Low pass filter:

For the series tuned low pass filter the impedance is:

\[
Z_{sh(h)} = \left[ R + j(hX_L - \frac{X_C}{h}) \right]
\]

\[
X_C = \frac{V_{ph}^2}{\omega_{sh} h}
\]

\[
X_L = \frac{X_C}{h^2}
\]

Where \( Q_{sh} = \) reactive power provided by the passive filter in VAR per phase, \( X_L = \) reactance of inductor, \( X_C = \) reactance of capacitor, \( h = \) harmonic order of the passive filter, \( V_{ph}=\) Phase voltage Initially the reactive power requirement is assumed to be 25% of the rating of the load. It may be equally divided into different filter branches. The value of series tuned element can be calculated from (4) and (5). The quality factor of the low pass filter is:

\[
QF = \frac{X_L}{R}
\]
Here the quality factor is assumed to 30 to calculate the value of the resistive element. The resonant frequency is given by

\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]  

(7)

Where \( R \) = filter resistance  
\( L \) = filter inductance  
\( C \) = filter capacitance

Quality factor can be expressed as

\[ QF = \frac{L}{R^2C} \]  

(11)

The design of passive shunt filter is carried out as per the reactive power requirements. The filter is designed to compensate the reactive power of the system. Hence the passive filter helps in maintaining the regulation of dc link voltage within limits and power factor improvement as improving the THD of supply current. It also sinks the harmonic currents of the frequencies at which the passive filter has been tuned. Depending on the harmonic spectrum of the supply current passive filter is designed for low pass filters which is tuned for 5\(^{th}\) and 7\(^{th}\) harmonic frequency and high pass filter which is tuned for 11\(^{th}\) harmonic frequency shown in Fig.3. In low pass filter Fig.4 R, L, and C are connected in series. The high pass filter Fig.5 consists of a capacitor which is connected in series with the parallel combination of the resistor and inductor to the converter. In this paper passive LC filter is designed for the 5\(^{th}\) and 7\(^{th}\) order harmonic frequency, and the filter component values are:

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Component Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>5(^{th})</td>
<td>( C = 11.24e^{-3} )</td>
</tr>
<tr>
<td>7(^{th})</td>
<td>( C = 15.7e^{-3} )</td>
</tr>
</tbody>
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**IV RESULT DISCUSSION**

Generally, it is important that the harmonic components of output voltage produced by inverter itself should be reduced to alleviate the output current ripple and the core loss of inductor. The developed inverter is simulated and the output voltages waveforms are represented. The figures given below represent the simulated results of output voltage and current for various modulation indexes from 0.2-0.9.
Figure 6: Grid phase voltage and Inverter current

Figure 7: multilevel outputs fed to a harmonic compensation

Figure 8: Line voltage after Compensation

Figure 9: Waveform and FFT analysis of a Grid Phase Voltage

In fig.8 shows the line voltage wave form after compensation. Total Harmonic Distortion of the grid phase voltage is calculated in the FFT analysis in the MATLAB software and the grid phase voltage before compensation is given as 40.33% which is abnormal THD under IEEE standards.

Figure 10: Multi level output fed to a Grid as a Shunt Active power and FFT analysis.
Figure 11: Waveform and FFT analysis Output after Compensation

Fig. 10 and 11 shows the multilevel output fed to a grid through shunt active filter and its corresponding THD level using FFT analysis and waveform after compensation gives THD of 0.12% which is in under IEEE 519 power quality condition.

V. CONCLUSION

Based on the proposed cascade multilevel inverter model, the feedback-control technique, called the decoupling power control, was first presented for the three-level cascaded-PWM inverter, and its performance and stability were verified by both computer simulations and experiments.

A new multilevel-voltage modulation technique, named the cascaded multilevel Inverter, was proposed to overcome the imbalance problem among the DC-capacitor voltages in the system, which minimizes the complexity of the main control loop and significantly improves the reliability of the entire control system. The seven-level cascaded multilevel inverter system was selected as an example in order to validate the proposed control system. By utilizing the cascaded Multilevel Inverter, all DC-capacitor voltages can be balanced in all operation conditions. Based on the philosophy behind the proposed technique, CMCs with any number of voltage levels can be modeled as three-level cascaded converters. This dramatically simplifies the entire control design process.

The THD of different methods are as shown in above table. For THD concerns, the proposed technique can be further extended to have more than one switching per line cycle in order to lower the THD at low modulation indices.

REFERENCES


